



STP3NB100 STP3NB100FP

N-CHANNEL 1000V - 5.3Ω - 3A TO-220/TO-220FP
PowerMesh™ MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{D(on)}	I _D
STP3NB100	1000 V	< 6 Ω	3 A
STP3NB100FP	1000 V	< 6 Ω	3 A

- TYPICAL R_{D(on)} = 5.3Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest R_{D(on)} per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP3NB100	STP3NB100FP	
V _{DS}	Drain-Source Voltage (V _{GS} = 0)	1000		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	1000		V
V _{GS}	Gate-source Voltage	±30		V
I _D	Drain Current (continuos) at T _C = 25°C	3	3 (*)	A
I _D	Drain Current (continuos) at T _C = 100°C	1.9	1.9 (*)	A
I _{DM} (▲)	Drain Current (pulsed)	12	12	A
P _{TOT}	Total Dissipation at T _C = 25°C	100	35	W
	Derating Factor	0.8	0.28	W/°C
dv/dt ⁽¹⁾	Peak Diode Recovery voltage slope	4.5	4.5	V/ns
V _{ISO}	Insulation Withstand Voltage (DC)	-	2500	V
T _{stg}	Storage Temperature	−65 to 150		°C
T _j	Max. Operating Junction Temperature	150		°C

(*)Pulse width limited by safe operating area

(*)Limited only by maximum temperature allowed

(1)I_{SD} ≤ 3A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

STP3NB100/FP

THERMAL DATA

		TO-220	TO-220FP	
Rthj-case	Thermal Resistance Junction-case Max	1.25	3.57	°C/W
Rthj-amb T _j	Thermal Resistance Junction-ambient Max Maximum Lead Temperature For Soldering Purpose	62.5 300		°C/W °C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	3	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	244	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	1000			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 1.5 A		5.3	6	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 1.7 A		2.8		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		700		pF
C _{oss}	Output Capacitance			80		pF
C _{rss}	Reverse Transfer Capacitance			8		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 500\text{ V}$, $I_D = 1.5\text{ A}$		18		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		12		ns
Q_g	Total Gate Charge	$V_{DD} = 800\text{V}$, $I_D = 3\text{ A}$,		22		nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 10\text{V}$		6		nC
Q_{gd}	Gate-Drain Charge			10.5		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(V_{off})}$	Off-voltage Rise Time	$V_{DD} = 800\text{V}$, $I_D = 3\text{ A}$,		22		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (see test circuit, Figure 5)		28		ns
t_c	Cross-over Time			30		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current			3		A
$I_{SDM}^{(1)}$	Source-drain Current (pulsed)			12		A
$V_{SD}^{(2)}$	Forward On Voltage	$I_{SD} = 3\text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 3\text{ A}$, $dI/dt = 100\text{A}/\mu\text{s}$,		580		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 100\text{V}$, $T_j = 150^\circ\text{C}$		2.9		μC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		10		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

STP3NB100/FP

Fig. 1: Unclamped Inductive Load Test Circuit

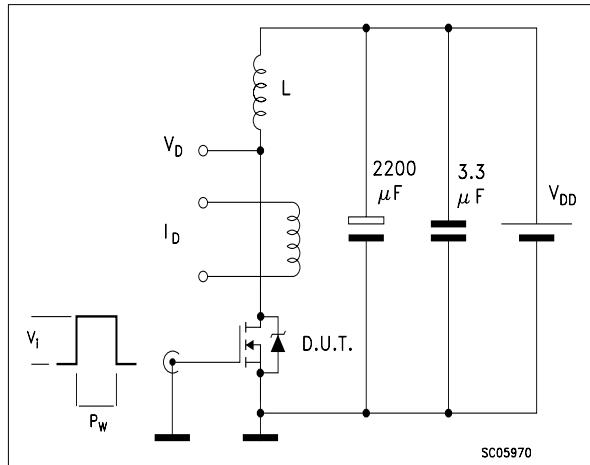


Fig. 2: Unclamped Inductive Waveform

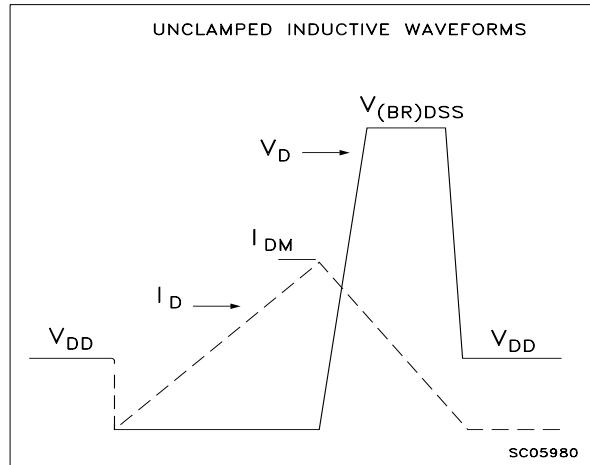


Fig. 3: Switching Times Test Circuit For Resistive Load

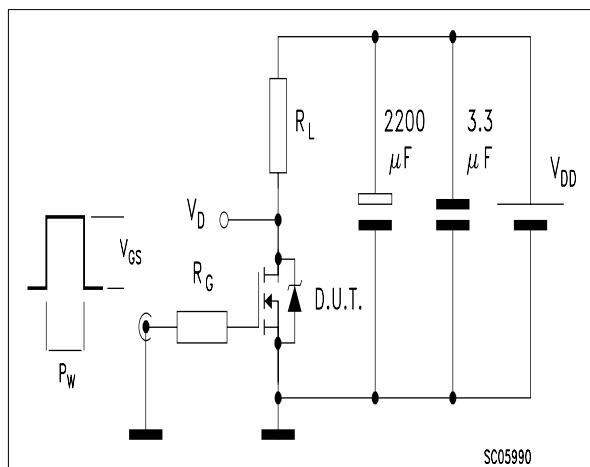


Fig. 4: Gate Charge test Circuit

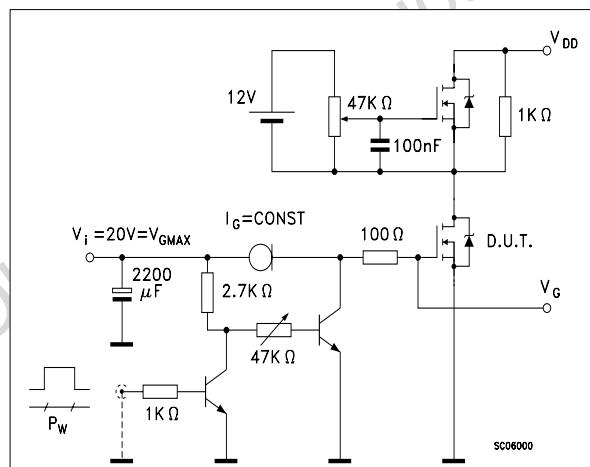
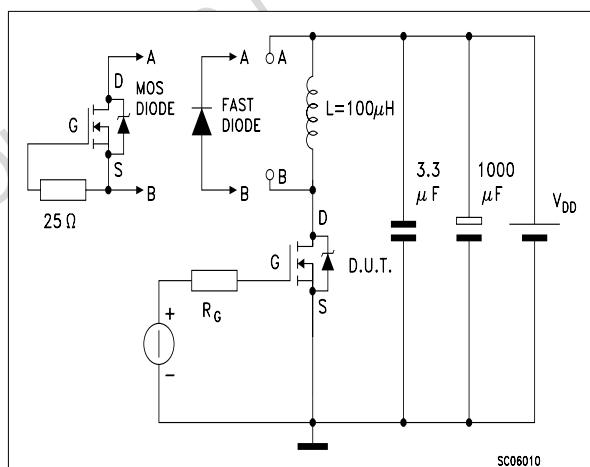
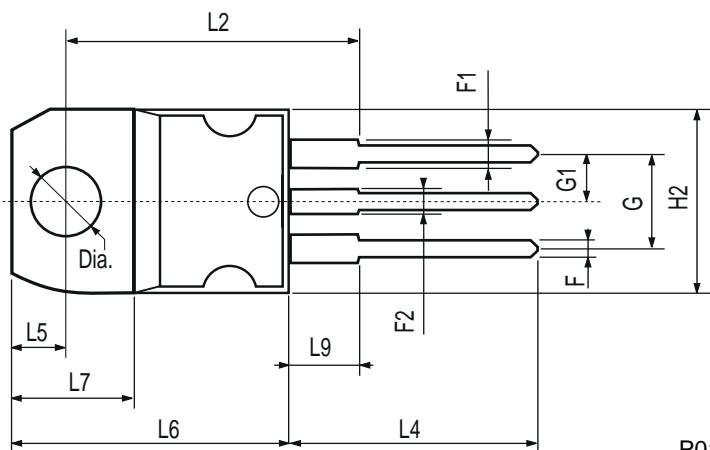
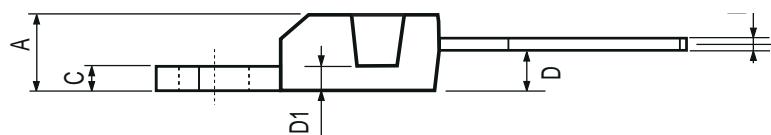


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



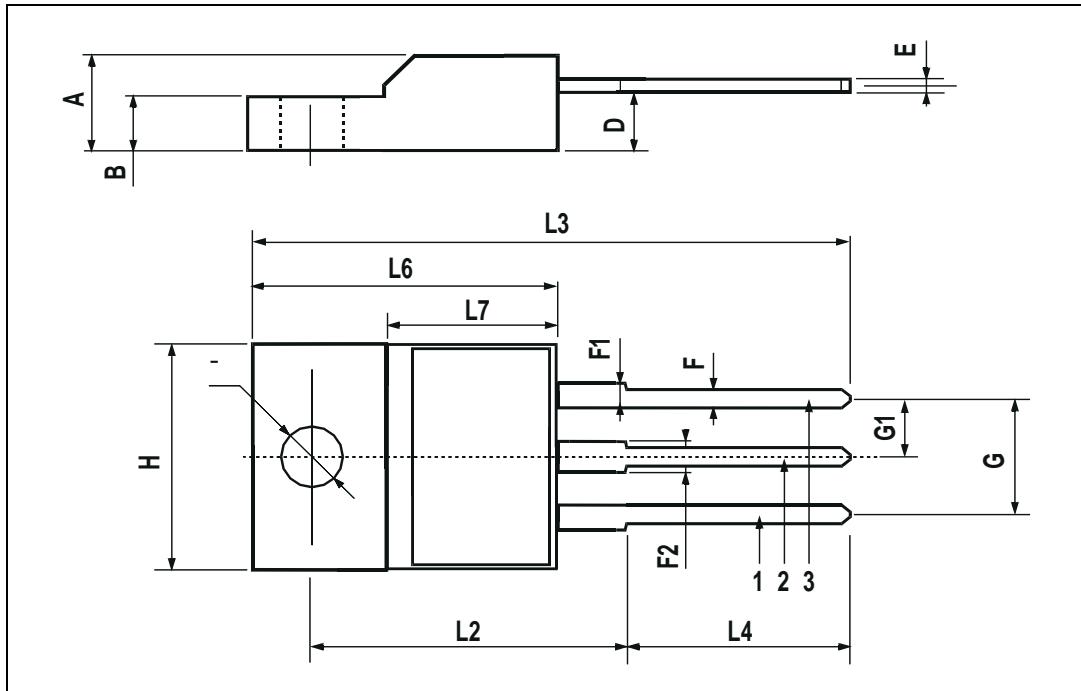
TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



TO-220FP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2000 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>