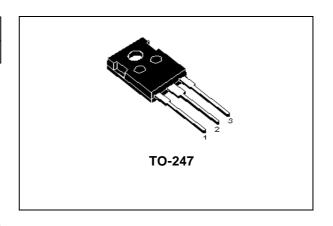


# **STW26NM60**

# N-CHANNEL 600V - 0.125Ω - 26A TO-247 Zener-Protected MDmesh™Power MOSFET

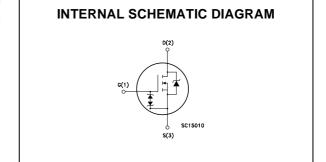
TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STW26NM60	600 V	< 0.135 Ω	30 A

- TYPICAL  $R_{DS}(on) = 0.125\Omega$
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- IMPROVED ESD CAPABILITY
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE



#### **DESCRIPTION**

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.



#### **APPLICATIONS**

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

#### ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STW26NM60	W26NM60	TO-247	TUBE

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#### **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	600	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	600	V
V <sub>GS</sub>	Gate- source Voltage	± 30	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	30	А
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	18.9	А
I <sub>DM</sub> (•)	Drain Current (pulsed)	120	А
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	313	W
	Derating Factor	2.5	W/°C
V <sub>ESD(G-S)</sub>	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	6000	V
dv/dt (1)	Peak Diode Recovery voltage slope	15	V/ns
T <sub>j</sub> T <sub>stg</sub>	Operating Junction Temperature Storage Temperature	-55 to 150	°C

<sup>(•)</sup> Pulse width limited by safe operating area

#### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.4	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose	300	°C

#### **AVALANCHE CHARACTERISTICS**

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max)	13	Α
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting $T_j = 25$ °C, $I_D = I_{AR}$ , $V_{DD} = 50$ V)	740	mJ

#### **GATE-SOURCE ZENER DIODE**

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
BV <sub>GSO</sub>	Gate-Source Breakdown Voltage	Igss=± 1mA (Open Drain)	30			V

#### PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

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<sup>(1)</sup>  $I_{SD} \leq 26A$ ,  $di/dt \leq 200A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_i \leq T_{JMAX}$ .

# **ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25^{\circ}C$ UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0$	600			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	$V_{DS}$ = Max Rating $V_{DS}$ = Max Rating, $T_{C}$ = 125 °C			10 100	μΑ μΑ
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20V			±10	μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\mu A$	3	4	5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	$V_{GS} = 10V, I_D = 13 A$		0.125	0.135	Ω

#### **DYNAMIC**

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> = 15 V <sub>,</sub> I <sub>D</sub> = 13 A		20		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$ , $f = 1 MHz$ , $V_{GS} = 0$		2900 900 40		pF pF pF

#### SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub>	Turn-on Delay Time Rise Time	$V_{DD} = 300 \text{V}, I_D = 13 \text{ A}$ $R_G = 4.7\Omega \text{ V}_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3)		35 22		ns ns
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V <sub>DD</sub> = 480V, I <sub>D</sub> = 26 A, V <sub>GS</sub> = 10V		73 20 37	102	nC nC nC

#### **SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
$\begin{matrix} t_{r(Voff)} \\ t_{f} \end{matrix}$	Off-voltage Rise Time Fall Time	$V_{DD} = 480 \text{V}, I_D = 26 \text{ A},$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{V}$		14 20		ns ns
t <sub>c</sub>	Cross-over Time	(Inductive Load see, Figure 5)		40		ns

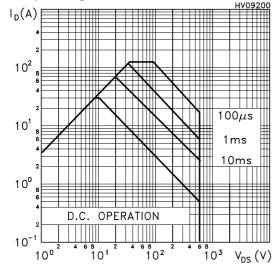
#### SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub> I <sub>SDM</sub> (2)	Source-drain Current Source-drain Current (pulsed)				26 104	A A
V <sub>SD</sub> (1)	Forward On Voltage	I <sub>SD</sub> = 26 A, V <sub>GS</sub> = 0			1.5	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD}$ = 26 A, di/dt = 100A/µs $V_{DD}$ = 100 V, $T_j$ = 25°C (see test circuit, Figure 5)		450 7 30.5		ns µC A
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD}$ = 26 A, di/dt = 100A/ $\mu$ s $V_{DD}$ = 100 V, $T_j$ = 150°C (see test circuit, Figure 5)		560 9 32.5		ns μC A

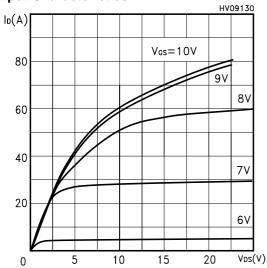
Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

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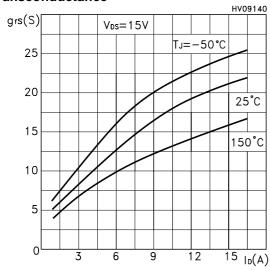
#### Safe Operating Area For TO-247



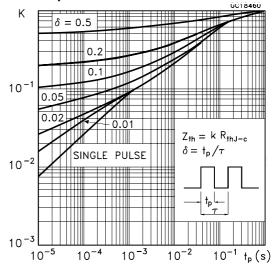
#### **Output Characteristics**



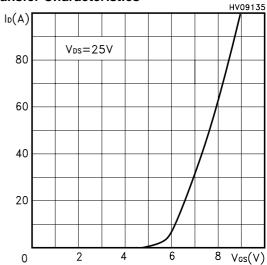
#### **Transconductance**



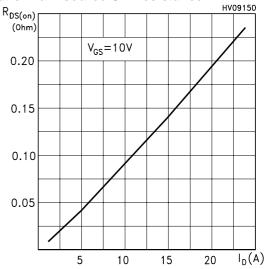
#### Thermal Impedance For TO-247



#### **Transfer Characteristics**

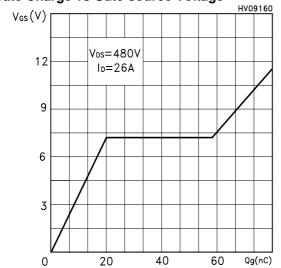


#### **Static Drain-source On Resistance**

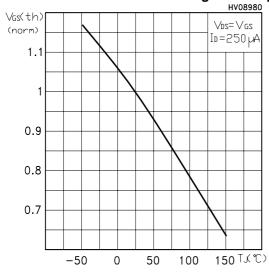


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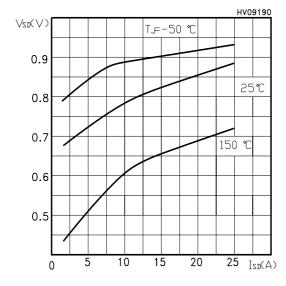
### **Gate Charge vs Gate-source Voltage**



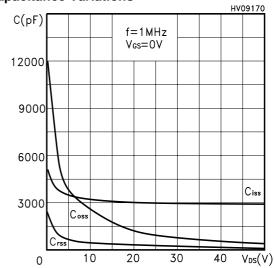
#### Normalized Gate Threshold Voltage vs Temp.



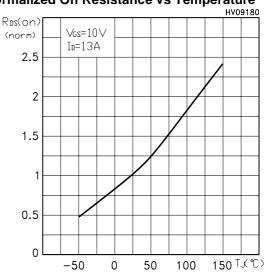
#### **Source-drain Diode Forward Characteristics**



#### **Capacitance Variations**



#### Normalized On Resistance vs Temperature



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Fig. 1: Unclamped Inductive Load Test Circuit

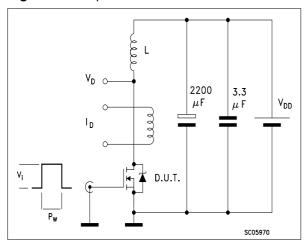


Fig. 3: Switching Times Test Circuit For Resistive Load

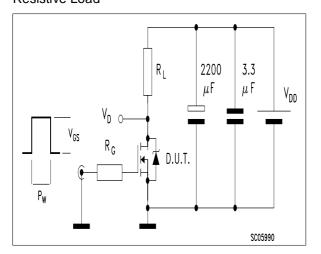


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

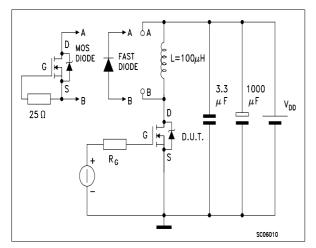


Fig. 2: Unclamped Inductive Waveform

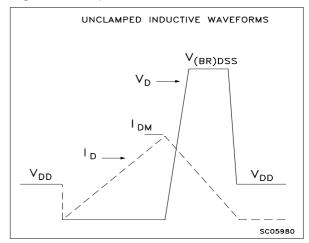
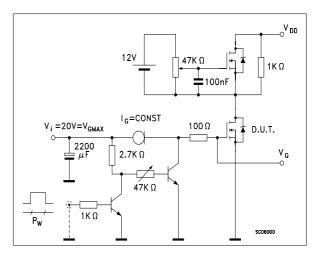


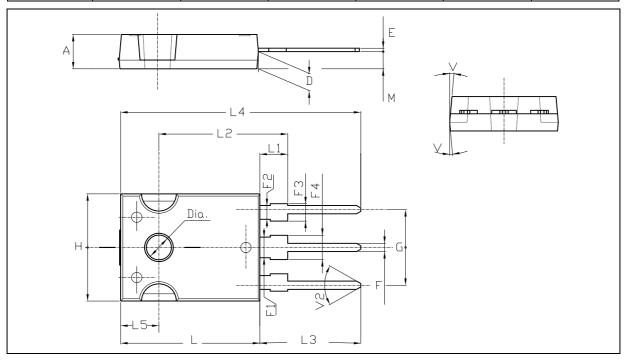
Fig. 4: Gate Charge test Circuit



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## **TO-247 MECHANICAL DATA**

DIM		mm.			inch	
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
А	4.85		5.15	0.19		0.20
D	2.20		2.60	0.08		0.10
E	0.40		0.80	0.015		0.03
F	1		1.40	0.04		0.05
F1		3			0.11	
F2		2			0.07	
F3	2		2.40	0.07		0.09
F4	3		3.40	0.11		0.13
G		10.90			0.43	
Н	15.45		15.75	0.60		0.62
L	19.85		20.15	0.78		0.79
L1	3.70		4.30	0.14		0.17
L2		18.50			0.72	
L3	14.20		14.80	0.56		0.58
L4		34.60			1.36	
L5		5.50			0.21	
М	2		3	0.07		0.11
V		5°			5°	
V2		60°			60°	
Dia	3.55		3.65	0.14		0.143



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