4V Drive Nch MOS FET 2SK2504

●Structure

Silicon N-channel MOS FET

● Features

- 1) Low On-resistance.
- 2) Fast switching speed.
- 3) Wide SOA (safe operating area).
- 4) 4V drive.
- 5) Drive circuits can be simple.
- 6) Parallel use is easy.

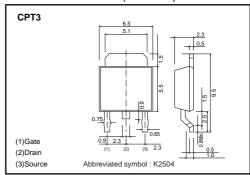
Applications

Switching

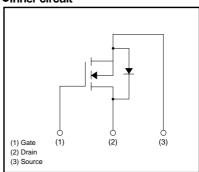
Packaging specifications

Туре	Package	Taping
	Code	TL
	Basic ordering unit (pieces)	2500
2SK2504		0

●External dimensions (Unit : mm)



•Inner circuit



● Absolute maximum ratings (Ta=25°C)

Paramete	Symbol	Limits	Unit	
Drain-source voltage		Voss	100	V
Gate-source voltage		Vgss	±20	V
Dunin augment	Continuous	lσ	5	Α
Drain current	Pulsed	IDP*	20	А
Reverse drain	Continuous	Idr	5	А
current	Pulsed	IDRP*	20	Α
Total power dissipation(Tc=25°C)		Pp	20	W
Channel temperature	!	Tch	150	°C
Storage temperature		Tstg	-55 to +150	°C

^{*} Pw \leq 10 μ s, Duty cycle \leq 1%

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Gate-source leakage	lgss	-	_	±100	nA	Vgs= ±20V, Vps=0V
Drain-source breakdown voltage	V(BR)DSS	100	_	_	V	In=1mA, Vgs=0V
Zero gate voltage drain current	IDSS	_	_	10	μΑ	VDS=100V, VGS=0V
Gate threshold voltage	VGS(th)	1.0	_	2.5	V	Vos=10V, Io=1mA
Static drain-source on-state	D	_	0.18	0.22	Ω	In=2.5A, Vgs=10V
resistance	RDS(on)	_	0.25	0.28		In=2.5A, Vgs=4V
Forward transfer admittance	Y _{fs} *	4.0	_	_	S	ID=2.5A, VDS=10V
Input capacitance	Ciss	_	520	_	pF	Vps=10V
Output capacitance	Coss	-	175	_	pF	Vgs=0V
Reverse transfer capacitance	Crss	_	60	_	pF	f=1MHz
Turn-on delay time	td(on)	_	5.0	_	ns	ID=2.5A, VDD≒50V
Rise time	tr	_	20	_	ns	Vgs=10V
Turn-off delay time	td(off)	_	50	_	ns	RL=20Ω
Fall time	tf	_	20	_	ns	R _G =10Ω

^{*} Pw \leq 300 μ s, Duty cycle \leq 1%

•Electrical characteristics curve

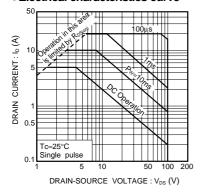


Fig.1 Maximum Safe Operating Area

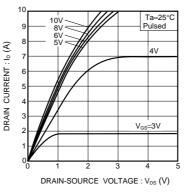


Fig.2 Typical Output Characteristics

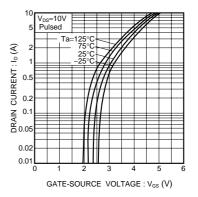


Fig.3 Typical Transfer Characteristics

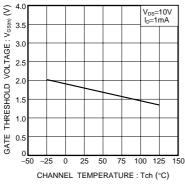


Fig.4 Gate Threshold Voltage vs. Channel Temperature

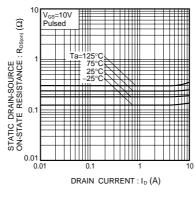


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (I)

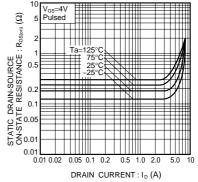


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (II)

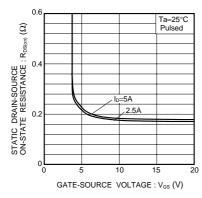


Fig.7 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

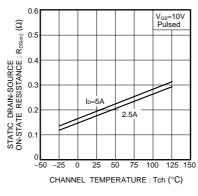


Fig.8 Static Drain-Source On-State Resistance vs. Channel Temperature

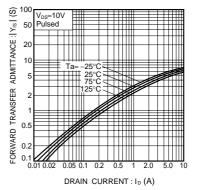


Fig.9 Forward Transfer Admittance vs. Drain Current

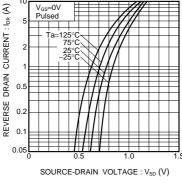


Fig.10 Reverse Drain Current vs. Source-Drain Voltage (I)

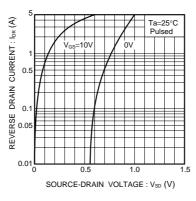


Fig.11 Reverse Drain Current vs. Source-Drain Voltage (II)

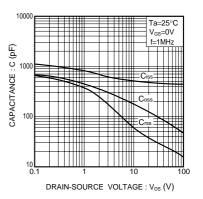


Fig.12 Typical Capacitance vs. Drain-Source Voltage

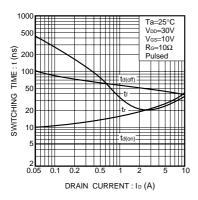


Fig.13 Switching characteristics (See Figures 16 and 17 for the measurement circuit and resultant waveforms)

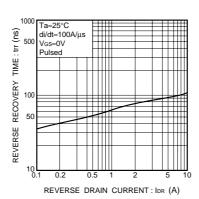


Fig.14 Reverse Recovery Time vs. Reverse Drain Current

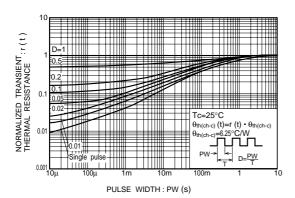
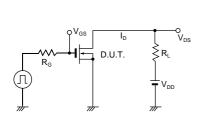


Fig.15 Normalized Transient Thermal Resistance vs. Pulse Width

•Switching characteristics measurement circuit



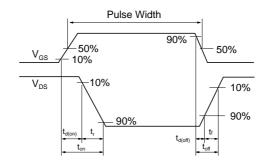


Fig.16 Switching Time Test Circuit

Fig.17 Switching Time Waveforms

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