

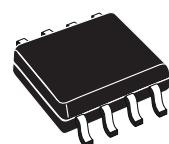


STS3DNE60L

DUAL N-CHANNEL 60V - 0.065Ω - 3A SO-8 STripFET™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STS3DNE60L	60 V	< 0.08 Ω	3 A

- TYPICAL R_{DS(on)} = 0.065Ω
- LOW THRESHOLD GATE DRIVE
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY



SO-8

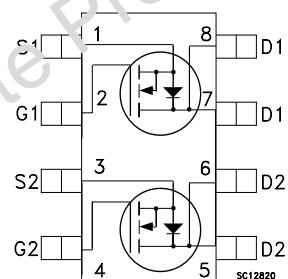
DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC MOTOR DRIVE
- DC-DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN PORTABLE/ DESKTOP PCs

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	60	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	60	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C Single Operation	3	A
	Drain Current (continuous) at T _C = 100°C Single Operation	1.9	A
I _{DM} (•)	Drain Current (pulsed)	12	A
P _{TOT}	Total Dissipation at T _C = 25°C Dual Operation Total Dissipation at T _C = 25°C Single Operation	1.6 2.0	W W

(•)Pulse width limited by safe operating area

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THERMAL DATA

R _{thj-amb}	(*)Thermal Resistance Junction-amb Max Single Operation (*)Thermal Resistance Junction-amb Max Dual Operation	62.5 78	°C/W °C/W
T _j T _{stg}	Max. Operating Junction Temperature Storage Temperature	150 – 55 to 150	°C °C

(*) Mounted on FR-4 Board (t ≤ 10 sec)

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	60			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 1.5 A V _{GS} = 4.5 V, I _D = 1.5 A		0.065 0.08	0.08 0.1	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 15V , I _D = 1.5 A		5		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		815 125 40		pF pF pF

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 30 \text{ V}$, $I_D = 3 \text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 5 \text{ V}$ (see test circuit, Figure 3)		20 30		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 24 \text{ V}$, $I_D = 3 \text{ A}$, $V_{GS} = 4.5 \text{ V}$		13.5 6 3.5		nC nC nC

SWITCHING OFF

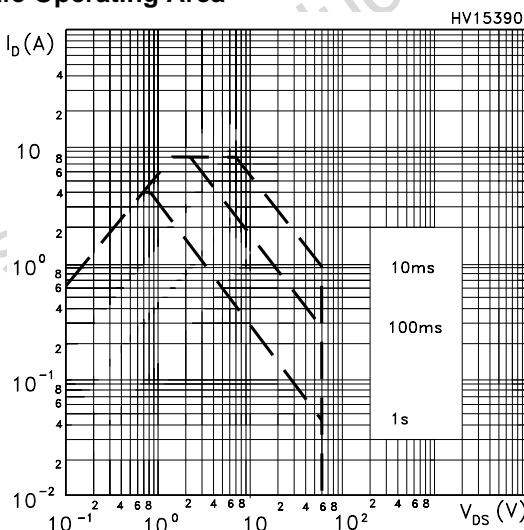
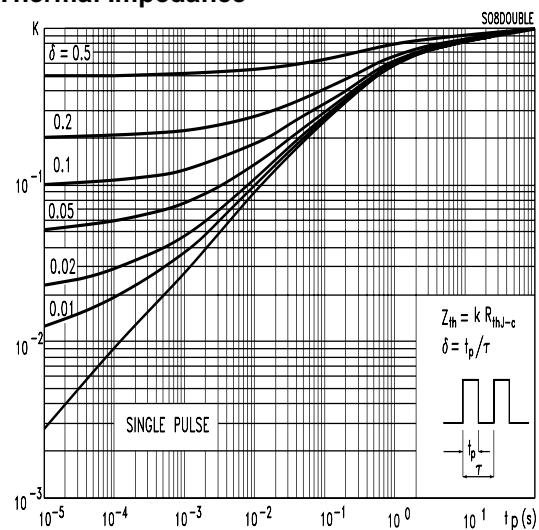
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{(off)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 48 \text{ V}$, $I_D = 3 \text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 5 \text{ V}$ (see test circuit, Figure 5)		12 16 32		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				3	A
I_{SDM} (1)	Source-drain Current (pulsed)				12	A
V_{SD} (2)	Forward On Voltage	$I_{SD} = 3 \text{ A}$, $V_{GS} = 0$			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 3 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 30 \text{ V}$, $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		60 130 4		ns nC A

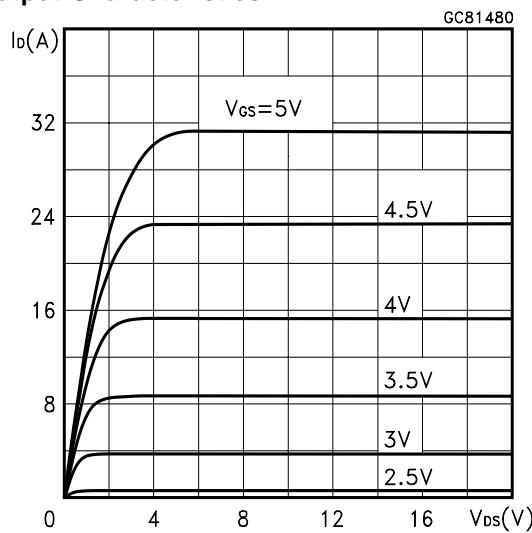
Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

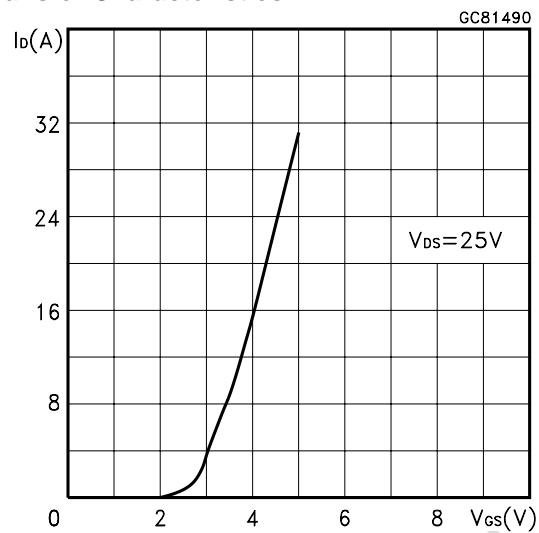
Safe Operating Area**Thermal Impedance**

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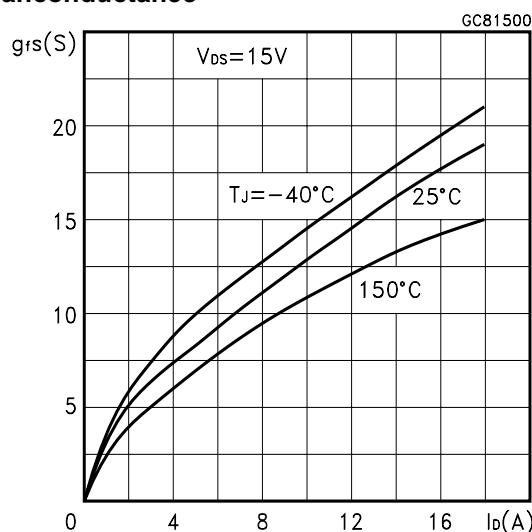
Output Characteristics



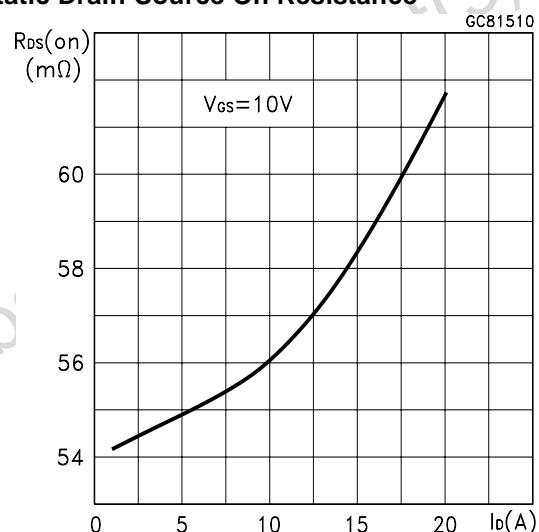
Transfer Characteristics



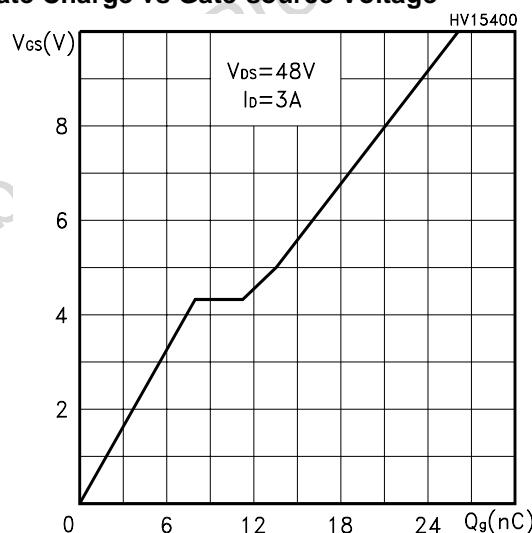
Transconductance



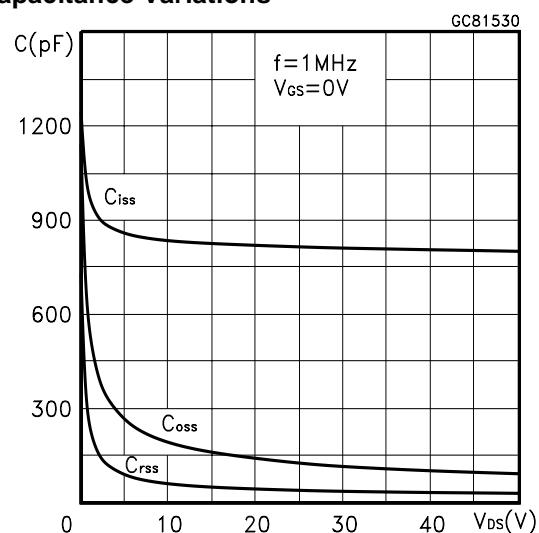
Static Drain-Source On Resistance

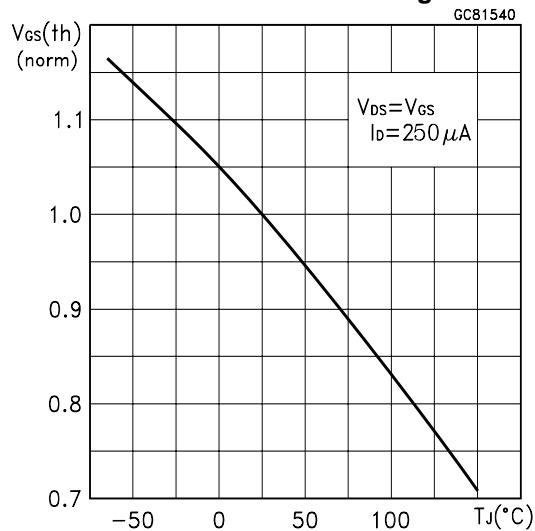
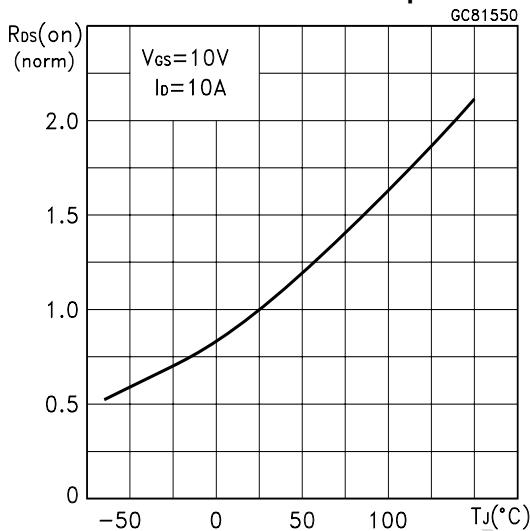
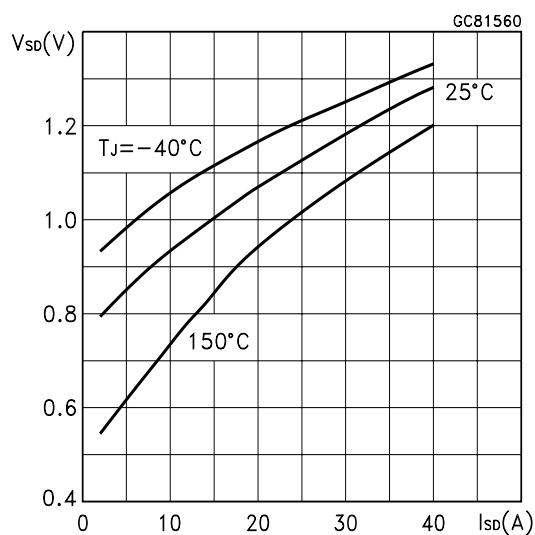


Gate Charge vs Gate-source Voltage



Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.**Normalized On Resistance vs Temperature****Source-drain Diode Forward Characteristics**

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Fig. 1: Unclamped Inductive Load Test Circuit

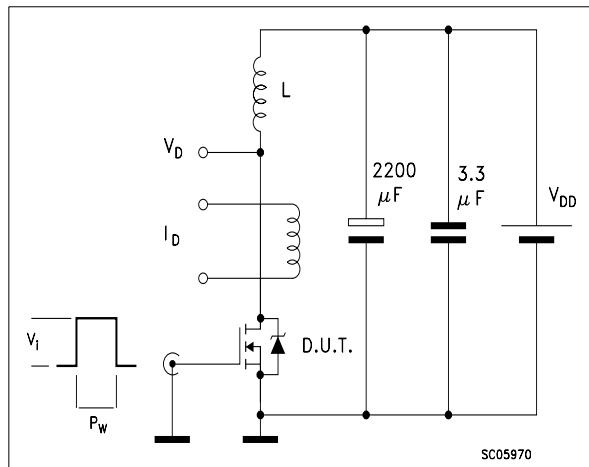


Fig. 2: Unclamped Inductive Waveform

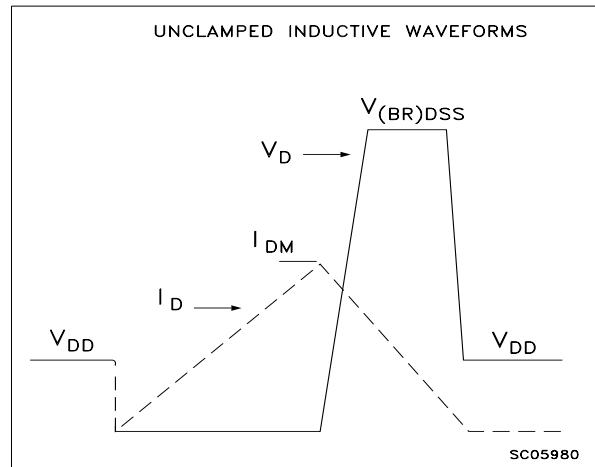


Fig. 3: Switching Times Test Circuit For Resistive Load

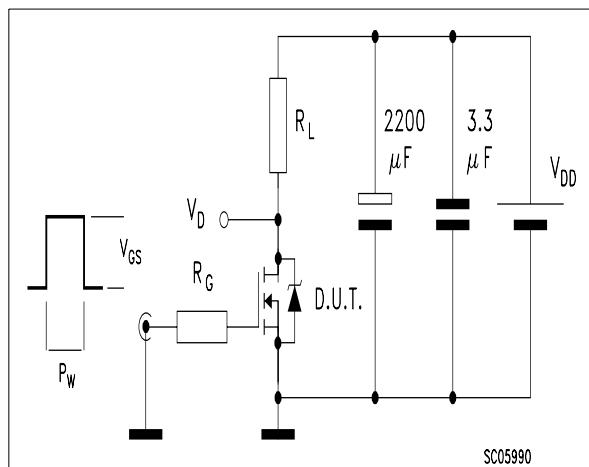


Fig. 4: Gate Charge test Circuit

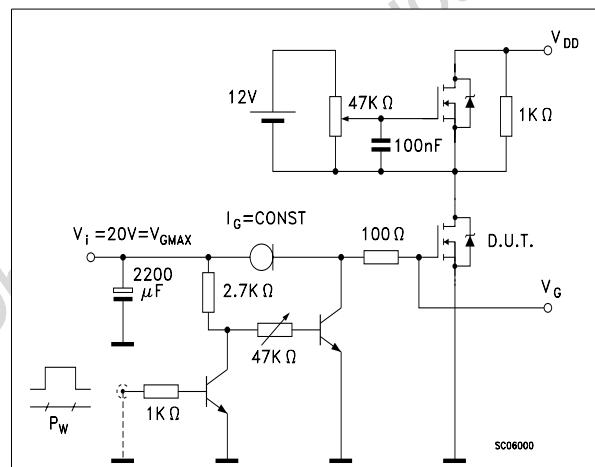
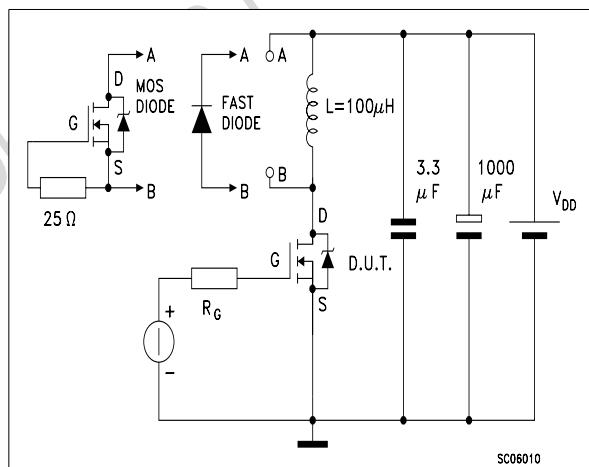
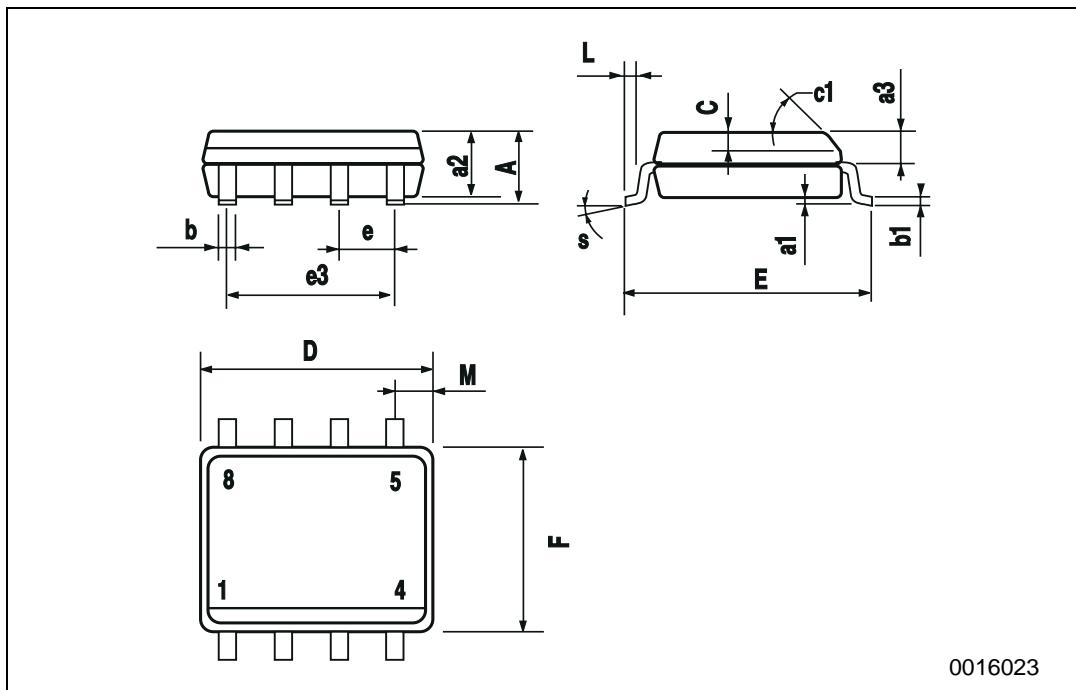


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1		45 (typ.)				
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S		8 (max.)				



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